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10/039,934	10/26/2001	Mohammed Ali AbdEl-Halim AbdEl-Wahid	1011-59137	9957

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KLARQUIST SPARKMAN, LLP
121 SW SALMON STREET
SUITE 1600
PORTLAND, OR 97204

EXAMINER	
TRIMMINGS, JOHN P	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,934	ABDEL-WAHID, MOHAMMED ALI ABDEL-HALIM	
	Examiner	Art Unit	
	John P Trimmings	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-36 are presented for examination.

Information Disclosure Statement

The examiner has considered the Information Disclosure Statement dated 4/29/2002.

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: FIG.2 95, FIG.5 370, and FIG.9 545 & 480. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: page 8 line 23 recites, "464, are BitByt...", but the examiner believes it should read, "464, and BitByt...". Appropriate correction is required.

3. The disclosure is objected to because of the following informalities: page 9 line 12 recites, "one bit is shifted in (310) from the CUT to the shift register 320,...", but the

examiner believes it should read, "one bit is shifted in (320) from the CUT to the shift register 310,...", Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claim 35 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Specifically, the claim recites selecting an alalog circuit which the claim types as being a filter. The examiner does not know what kind of filter the applicant has in mind that would qualify to be an analog circuit, and the specification does not teach this circuit.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim limits the memory to a programmable memory, but

the examiner is not sure what the applicant means by this claim. The memory may be a programmable read-only memory, but may also be any memory that stores data that may be programmable. The examiner needs clarification from the applicant.

6. Claim 10, dependent on Claim 1, recites the limitation "a second test controller module" in line 2. There is insufficient antecedent basis for this limitation in the claim, because there is no antecedent test controller in Claim 1.

7. Claim 34 recites the limitation "the comparing" in line 2. There is insufficient antecedent basis for this limitation in the claim.

8. Claim 35 recites the limitation "the selected analog circuit" in line 9. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 35 recites the limitation "the group" in line 9. There is insufficient antecedent basis for this limitation in the claim.

10. Claim 36 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The claim limits the method further by “transmitting instructions for generating testing circuitry”, but the examiner is not sure what the applicant means by this phrase. Literally, it may mean that there is claimed; a method that sends instructions on how to create circuitry for testing, but the examiner would like the applicant to more clearly state this limitation.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

11. Claims 17-19, 27-29, and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Sugamori, U.S. Patent No. 6536006.

As per Claim 17:

Sugamori teaches a method based on a system for testing a mixed signal integrated circuit having multiple analog nodes and testing circuitry (see Abstract), comprising: selecting an analog node in the integrated circuit from a list of analog nodes (column 8 lines 39-49) stored in a memory (FIG.4 41); obtaining a test value from the selected analog node (column 9 lines 21-23); retrieving a tolerance value associated with the selected analog node from a memory (column 8 lines 13-18 and lines 61-67); and comparing the test value of the selected analog node with the tolerance value (column 9 lines 23-30).

As per Claim 18:

Sugamori further teaches the method of claim 17 wherein the associated tolerance value is retrieved from the same memory (FIG.4 41) in which the list of analog nodes is stored.

As per Claim 19:

Sugamori further teaches the method of claim 17, wherein the comparing comprises checking whether the test value of the selected analog node is within the associated tolerance value (column 8 lines 21-29).

As per Claim 27:

Sugamori further teaches the method of claim 17, wherein the obtaining is responsive to stimuli transmitted to the integrated circuit from a location outside the integrated circuit (column 7 lines 56-63).

As per Claim 28:

Sugamori further teaches the method of claim 17 further comprising: prior to the comparing, selecting a condition checker in the testing circuitry for performing the comparing (column 8 lines 39-49).

As per Claim 29:

Sugamori further teaches the method of claim 17 further comprising, prior to the selecting: storing data identifying the analog nodes of the integrated circuit in a program memory in the testing circuitry (column 8 lines 39-49); storing tolerance values associated with the analog nodes of the integrated circuit in the program memory (column 8 lines 61-67).

As per Claim 36:

Sugamori teaches a computer-implemented method based on a test system, comprising: transmitting instructions for generating testing circuitry (column 12 lines 62-64) which includes: instructions for selecting an analog node from a list of analog nodes (column 8 lines 39-49) stored in a memory of an integrated circuit (column 8 lines 50-

60); obtaining a test value from the selected analog node (FIG.4 61); retrieving a tolerance value associated with the selected analog node from a memory (column 8 lines 50-67); and comparing the test value of the selected analog node with the tolerance value (column 9 lines 23-30).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

13. Claims 1-7, 9-11, 13-16, 30 and 33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugamori, U.S. Patent No. 6536006.

As per Claim 1:

Sugamori teaches a test system comprising testing circuitry (FIG.4 43) and core logic circuitry (FIG.4 19, 48), comprising: a memory that stores data identifying analog

nodes in the core logic circuitry and tolerance values associated with the analog nodes (FIG.4 68 and 60); a condition checker that compares actual test values of the analog nodes with the associated tolerance values (FIG.4 61); and a main control unit coupled to the memory and the condition checker (FIG.4 47) that synchronizes testing of the core logic circuitry. Sugamori however does not teach the above features as all being part of an integrated circuit, rather the system is composed of a tester board plus filter and the CUT and consists of two separate units. But it would have been obvious to one with ordinary skill in the art at the time of the invention, to combine the system into one integrated circuit, because it would have been an obvious design choice. And one would have been motivated by cost and speed of test to integrate the system of Sugamori, in the same manner that all improvements and miniaturizations occur every day in the art of integrated circuits. The applicant is directed to in re Larson, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965), where the court affirmed the rejection, holding "that the use of a one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice.", and in view of in re Larson, the claim is rejected.

As per Claim 2:

Sugamori further teaches the integrated circuit of claim 1 wherein the testing circuitry enables analog testing for on-line, off-line, and interactive field testing. The circuits arrangement can communicate on-line, as in the digital interfacing with the Tester Controller (FIG.4 43_2 to 41), or interactively between the Tester Controller (FIG.4 41) and the Event Tester (FIG.4 43_1), and then after storing instructions in the

Processor (FIG.4 67) the arrangement can fully test the CUT in an off-line basis (column 14 lines 5-13).

As per Claim 3:

Sugamori further teaches the integrated circuit of claim 1 wherein the testing circuitry further comprises a tester interface (FIG.4 53).

As per Claim 4:

Sugamori further teaches the integrated circuit of claim 3 wherein the tester interface is a host computer interface (FIG.4 64, System Bus).

As per Claim 5:

Sugamori further teaches the integrated circuit of claim 1 wherein the testing circuitry further comprises a second memory for storing diagnostic data (FIG.4 57).

As per Claim 6:

Sugamori further teaches the integrated circuit of claim 1 wherein the memory is located in the testing circuitry (FIG.4 68 and 60).

As per Claim 7:

Sugamori further teaches the integrated circuit of claim 1 wherein the memory is a programmable memory (FIG.4 68 or 60).

As per Claim 9:

Sugamori further teaches the integrated circuit of claim 1 wherein the testing circuitry includes a test controller module (FIG.4 43_1) comprising: a memory for storing data transmitted to the test controller module (FIG.4 68); a control unit (FIG.4 67); and a test access port controller (FIG.4 53 and column 8 lines 39-49).

As per Claim 10:

Sugamori further teaches the integrated circuit of claim 1 wherein the testing circuitry further comprises a second test controller module (FIG.4 43_2).

As per Claim 11:

Sugamori further teaches the integrated circuit of claim 1 wherein the condition checker (FIG.4 61) comprises: means for receiving the test values from the analog nodes (FIG.4 48), means for receiving the associated tolerance values (FIG.4 47); and means for checking whether the test values are within the associated tolerance values (column 9 lines 23-30).

As per Claim 13:

Sugamori further teaches the integrated circuit of claim 1 wherein the testing circuitry further comprises a second condition checker (FIG.4 66_2).

As per Claim 14:

Sugamori further teaches the integrated circuit of claim 1 wherein the main control unit comprises: a program counter (column 8 lines 61-67); a plurality of registers for storing addresses of analog nodes (FIG.4 68 and 60); and a control unit (FIG.4 67).

As per Claim 15:

Sugamori further teaches the integrated circuit of claim 14 wherein the main control unit further comprises: a data pointer (FIG.5 58) for addressing a memory to archive test results (FIG.5 57 and column 8 lines 12-13).

As per Claim 16:

Sugamori further teaches the integrated circuit of claim 14, wherein the testing circuitry comprises a plurality of condition checkers (FIG.4 66_1, 66_2, etc), and wherein the main control unit further comprises: means for selecting a condition checker from the plurality of condition checkers in the testing circuitry (FIG.4 53 and column 8 lines 39-49) to compare a test value with an associated tolerance value (column 9 lines 23-30).

As per Claim 30:

Sugamori teaches a test system comprising testing circuitry and core logic circuitry, wherein the testing circuitry comprises: means for selecting an analog node in the core logic circuitry from a list of analog nodes stored in a memory (column 8 lines 39-49); means for obtaining a test value from the selected analog node (column 8 lines 50-60); means for retrieving a tolerance value associated with the selected analog node from a memory (column 8 lines 61-67); and means for checking whether the test value of the selected analog node is within the associated tolerance value (column 9 lines 23-30). Sugamori however does not teach the above features as all being part of an integrated circuit, rather the system is composed of a tester board plus filter and the CUT and consists of two separate units. But it would have been obvious to one with ordinary skill in the art at the time of the invention, to combine the system into one integrated circuit, because it would have been an obvious design choice. And one would have been motivated by cost and speed of test to integrate the system of Sugamori, in the same manner that all improvements and miniaturizations occur every day in the art of integrated circuits. The applicant is directed to in re Larson, 340 F.2d 965, 968, 144

USPQ 347, 349 (CCPA 1965), where the court affirmed the rejection, holding "that the use of a one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice.", and in view of in re Larson, the claim is rejected.

As per Claim 33:

Sugamori further teaches the integrated circuit of claim 30 further comprising a means for communicating with a host computer (FIG.4 67, 53 to 41).

As per Claim 34:

Sugamori further teaches the integrated circuit of claim 30 further comprising: a means for selecting a condition checker for performing the comparing (column 8 lines 39-49).

As per Claim 35:

Sugamori teaches a method based on a system for testing an integrated circuit having multiple analog nodes and testing circuitry (see Abstract), the method comprising: selecting an analog node in the integrated circuit from a list of analog nodes stored in a memory in the testing circuitry (column 8 lines 39-60); obtaining a test value from the selected analog node (FIG.4 61); retrieving a tolerance value associated with the selected analog node from a memory in the testing circuitry (column 8 lines 50-67); and comparing the test value of the selected analog node with the tolerance value (column 9 lines 23-30); wherein the selected analog circuit is of a type selected from the group including at least: an analog-to-digital converter, a digital-to-analog converter, and a filter (column 3 lines 6-11 and FIG.4 48). Sugamori however does not teach the above

features as all being part of an integrated circuit, rather the system is composed of a tester board plus filter and the CUT and consists of two separate units. But it would have been obvious to one with ordinary skill in the art at the time of the invention, to combine the system into one integrated circuit, because it would have been an obvious design choice. And one would have been motivated by cost and speed of test to integrate the system of Sugamori, in the same manner that all improvements and miniaturizations occur every day in the art of integrated circuits. The applicant is directed to in re Larson, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965), where the court affirmed the rejection, holding "that the use of a one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice.", and in view of in re Larson, the claim is rejected.

14. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugamori, U.S. Patent No. 6536006, and further in view of Morris, U.S. Patent No. 5577052. Sugamori teaches the integrated circuit of claim 1 but fails to teach that the testing circuitry is JTAG-compliant. In an analogous art, Morris does teach this feature in column 9 lines 54-67 and column 10 lines 1-5. And Morris, in column 3 lines 64-67 and column 4 lines 1-8, recites the advantage of a mixed signal capable test system with reusable test program capabilities, applied to embedded circuits. One with ordinary skill in the art would apply the teachings of Morris to the test system of Sugamori in order to test embedded mixed signal circuits. Motivation for such a combination would be derived through Morris as suggested by the advantages above.

15. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sugamori, U.S. Patent No. 6536006, and further in view of Sunter et al., U.S. Patent No. 5659312. Sugamori further fails to teach the integrated circuit of claim 11 wherein the condition checker further comprises noise calibration circuitry. But Sunter et al. in an analogous art, teaches this feature in column 1 lines 40-43, column 2 lines 46-50, and column 11 lines 58-63. One with ordinary skill would combine the teaching of Sunter et al. to the test system of Sugamori in order to measure noise and other characteristics of a circuit under test. And Sunter et al., in column 2 lines 46-63 boasts of simple circuitry to test mixed signal circuits. One with ordinary skill in the art at the time of the invention, motivated as suggested by the advantage stated, would combine the references.

16. Claims 20-26 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugamori, U.S. Patent No. 6536006, and in view of Turnquist et al., U.S. Patent No. 6532561.

As per Claims 20 and 31:

Sugamori fails to further teach the method of claim 19 further comprising generating an error indication signal in response to the checking. But in an analogous art, Turnquist et al. does store an error signal in a latch (FIG.8 106) after checking the signal for a fault. One with ordinary skill would combine the circuit of Turnquist et al. in oder to compress the error reporting in the test system of Sugamori. Advantages to Turnquist et al. (column 2 lines 38-65) such as compression in an event based test system, would motivate one with ordinary skill in the art at the time of the invention to combine these references.

As per Claim 21:

Sugamori further teaches the method of claim 20 further comprising: reconfiguring a memory in the integrated circuit (FIG.4 57) to be operable to store diagnostic data from the testing circuitry (column 8 lines 21-25). And in view of the motivation previously stated, the claim is rejected.

As per Claim 22:

Sugamori further teaches the method of claim 21 further comprising: storing data identifying the selected analog node in the memory (column 8 lines 39-60); and storing the test value of the selected analog circuit in the memory (column 8 lines 61-67). And in view of the motivation previously stated, the claim is rejected.

As per Claim 23:

Sugamori further teaches the method of claim 20 further comprising: storing data identifying the selected analog node in a data memory in the testing circuitry (FIG.4 53 and 68); and storing the test value of the selected analog circuit in a data memory in the testing circuitry (FIG.4 60).

As per Claim 24:

Sugamori further teaches the method of claim 23 wherein the data identifying the selected analog node and the test value of the selected analog circuit are stored in the same data memory (FIG.4 68).

As per Claim 25:

Sugamori further teaches the method of claim 24 further comprising: obtaining a test value of a second analog node (FIG.4 66_2), wherein the second analog node is

associated with the selected analog node (fig4 43_1); storing data identifying the second analog node in the data memory (FIG.4 68); and storing the test value of the second analog node in the data memory (FIG.4 68).

As per Claim 26:

Sugamori further teaches the method of claim 24 further comprising uploading the contents of the data memory to a host computer (column 8 lines 39-60).

As per Claim 32:

Sugamori further teaches the integrated circuit of claim 30 further comprising: a means for storing data identifying the selected analog node in a data memory (FIG.4 53 and 68); and a means for storing the test value of the selected analog node in a data memory (FIG.4 68 and 57).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P Trimmings whose telephone number is 703-305-0714. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2133

jpt

Guy J. Lamarre
for
Albert DeCady
Primary Examiner